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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/664,585	09/17/2003	Hiroshi Masuya	81751.0066	3682

26021 7590 11/15/2006

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EXAMINER	
IM, JUNGHWA M	

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 11/15/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/664,585	MASUYA, HIROSHI	
	Examiner	Art Unit	
	Junghwa M. Im	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 August 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,5-7,9-11 and 21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,5-7,9-11 and 21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *17 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on August 6, 2006 has been entered.

Claim Objections

2. Claims 1 and 21 are objected to because of the following informalities:

Claims 1 and 21 recite the limitation "the sloping end section" without sufficient antecedent basis.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1, 6 and 9-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tsai (US Pat. 6,831,352) in view of Lee (US Pat. 6,157,074).

Regarding claim 1, Fig. 9B of Tsai shows a semiconductor device comprising:

a die pad (304 in Fig. 10);

a semiconductor chip (52) having an electrode (top of the semiconductor 52 where the wire 94 is connected) and bonded to the die pad;

an inner lead (310, 314, 312) having an end section (314) that is sloping upward and outward from the semiconductor chip wherein a surface of the die pad which the semiconductor chip is bonded faces upward;

a wire (316) electrically connecting the inner lead to the electrode;

a sealing section (322) sealing the inner lead, the semiconductor chip, and the wire; and

an outer lead (an extension of the inner lead 312) extending outward from the sealing section; and

wherein a portion of the inner lead (312) is higher than the semiconductor chip.

Fig. 9B of Tsai shows most aspects of the instant invention except "the wire is bonded to the sloping end section of the inner lead." Fig. 4 of Lee shows a semiconductor package wherein a wire (30) is bonded to the end section of the inner lead (36) that is sloping upward and outward from the semiconductor chip.

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to incorporate the teachings of Lee into the device of Tsai in order to have the wire bonded to the end section of the inner lead that is sloping upward and outward to increase the bonding strength of the wire to the lead.

Regarding claim 6, Fig. 9B of Tsai shows the inner lead further has a portion (312) extending in a horizontal direction and connected to the outer lead.

Regarding claim 9, Fig. 9B of Tsai shows a surface of the die pad (324) opposite to the semiconductor chip is exposed from the sealing section.

Regarding claim 10, Tsai discloses a circuit board on which the semiconductor device is mounted (column 1, lines 56-58).

Regarding claim 11, Tsai discloses that an electronic instrument comprising the semiconductor device as defined in claim 1 (column 2, lines 24-29).

5. Claims 1, 5, 7 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ishitsuka et al. (US Pat. 5,291,059), hereinafter Ishitsuka in view of Kuribayashi (Japanese Patent Pub. 10-150066)

Regarding claim 1, Fig. 1 of Ishitsuka shows a semiconductor device comprising:

a die pad (11);

a semiconductor chip (12) having an electrode (top of the semiconductor 12 where the wire 13 is connected) and bonded to the die pad;

an inner lead (14f, 14b, 14d) having an end section (14f) extending outward from the semiconductor chip wherein a surface of the die pad which the semiconductor chip is bonded faces upward;

a wire (13) electrically connecting the inner lead to the electrode;

a sealing section (15) sealing the inner lead, the semiconductor chip, and the wire; and

an outer lead (14e, 14a) extending outward from the sealing section;

wherein the wire is bonded to the end section of the inner lead, and

wherein a portion of the inner lead (14f) is higher than the semiconductor chip..

Fig. 1 of Ishitsuka shows most aspects of the instant invention except the inner lead having an end section (the beginning portion of the inner lead) that is sloping upward and outward from the semiconductor chip. Fig. 3 of Kuribayashi shows a semiconductor package wherein the end section of the inner lead (13; the beginning portion of the inner lead 12) is sloping upward and outward from the semiconductor (2).

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to incorporate the teachings of Kuribayashi into the device of Ishitsuka in order to have the end section of the inner lead (the beginning portion of the inner lead 14f) sloping upward and outward from the semiconductor, therefore, resulting in the wire bonded to the sloping end section to prevent short-circuiting during resin encapsulation (Abstract).

Regarding claim 5, Fig. 1 of Ishitsuka shows that the inner lead further has a sloping portion (14b) sloping down ward and outward from a higher end of the end section that is sloping.

Regarding claim 7, Fig. 3 of Kuribayashi shows a bonding position between the wire and the inner lead is lower than the position of the electrode (23).

Regarding claim 21, Fig. 1of Ishitsuka shows a semiconductor device comprising:

an inner lead (14f, 14b, 14d) having an end section (the beginning portion of the inner lead) extending outward from the semiconductor chip, the inner lead having a sloping portion (14b) downward and outward from the end of the end section (the beginning portion of the inner lead), wherein a surface of the die pad which the semiconductor chip is bonded faces upward;

a die pad (11);

a semiconductor chip (12) having an electrode (top of the semiconductor 12 where the wire 13 is connected) and bonded to the die pad;

a wire (13) electrically connecting the inner lead to the electrode;

a sealing section (15) sealing the inner lead, the semiconductor chip, and the wire; and

an outer lead (14e, 14a) extending outward from the sealing section, and

wherein a portion of the inner lead (14f) is higher than the semiconductor chip.

Fig. 1 of Ishitsuka shows most aspects of the instant invention except the inner lead having an end section (the beginning portion of the inner lead) that is sloping upward and outward from the semiconductor chip. Fig. 3 of Kuribayashi shows a semiconductor package wherein the end section (13; the beginning portion of the inner lead 12) is sloping upward and outward from the semiconductor (2).

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to incorporate the teachings of Kuribayashi into the device of Ishitsuka in order to have the end section (the beginning portion of the inner lead 14f) sloping upward and outward from the semiconductor to prevent short-circuiting during resin encapsulation (Abstract).

Response to Arguments

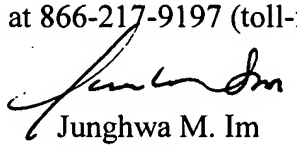
6. Applicant's arguments with respect to pending claims have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Junghwa M. Im whose telephone number is (571) 272-1655. The examiner can normally be reached on MON.-FRI. 8:30AM-5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie C. Lee can be reached on (571) 272-1732. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Junghwa M. Im
Examiner
Art Unit 2811

jmi
9/16/2006